REMARKS

This amendment is a full and timely response to the Non-Final Office Action dated August 2, 2011. Claims 1-6 are pending, with claims 1, 3, and 5 being independent.

In this amendment, claims 7-9 have been added. Support for these amendments is variously found in Applicant's specification as filed, including but not necessarily limited to the paragraphs ¶¶ [0043]-[0046] of the specification, as represented in U.S. Pub. No. 2006/0152461 A1. Reconsideration and allowance is requested in view of the following remarks. *No new matter has been added by these amendments.*

Claims 1-6 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over *Edwards*, U.S. Patent Number 6,498,438 (*Edwards*) in view of *Tusuchi*, WIPO No. 01/95596 (*Tusuchi*) - of which U.S. Patent Number 7,0985,991 was used as the English translation. This rejection is respectfully traversed.

Edwards discloses a circuit 40 for producing an output current (at output 50) from an input word using switching transistors and for managing, via a transistor 70 in FIG. 6 (or T1 in FIG. 8), this output current. *Edwards* also discloses avoiding a large voltage ramp at output 50 using a four transistor arrangement (T2 – T5) when resetting the voltage. (*Edwards*, FIGs. 4-5c and 7d-8).

Independent claim 1, as amended, recites "[*a*] *method for operating a constant current circuit, comprising: after connecting a sampling capacitor connected between a gate and a source of a first transistor and a drain of the first transistor to a reference current source and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source, cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a buffer circuit, and driving the buffer circuit by a current of the first transistor due to the voltage between the gate and the source that is set in the sampling capacitor, wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source, a second signal that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor, a third signal to a gate of a*

fourth transistor connected between the drain of the first transistor and the buffer circuit, said setting the voltage across the sampling capacitor and said cutting off the connection occur within a precharge period to cause the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period, and the buffer circuit includes an analog buffer circuit and a precharge circuit; and executing a precharge processing for the precharge period by disconnecting the precharge circuit for the precharge period from the analog buffer circuit, where the buffer circuit transistor of the buffer circuit is part of the analog buffer circuit."

Edwards fails to disclose or suggest these claimed features. Specifically, Edwards fails to disclose "*cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a buffer circuit, and driving the buffer circuit by a current of the first transistor due to the voltage between the gate and the source that is set in the sampling capacitor.*" (Consistently, the Office Action on page 4 admits that *Edwards* does not disclose "a buffer circuit for driving the signal lines by an output circuit from digital-to-analog conversion circuit.")

Further, Applicant's features of "*said setting the voltage across the sampling capacitor and said cutting off the connection occur within a precharge period to cause the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period*" is not disclosed by *Edwards*. That is, the Office Action states that *Edwards* in FIG. 11 discloses "the charging of a capacitor prior to the output enable being applied and can be considered a pre-charge period." However, even if (but not admitted) the charging of the capacitor 72 of *Edwards* could be construed as a precharge period, *Edwards* still lacks the temporary connection as claimed and most certainly fails to disclose temporarily connecting the constant current circuit to a source of an output buffer and circuit transistor, as claimed by Appiocant.

Furthermore, Applicant's features of "*wherein the buffer circuit includes an analog buffer circuit and a precharge circuit,*" and "*executing a precharge processing for the precharge period by disconnecting the precharge circuit for the precharge period from the analog buffer circuit, where the buffer circuit transistor of the buffer circuit is part of the analog buffer circuit,*" are not disclosed by *Edwards*.

In addition, the Office Action admits that *Edwards* does not disclose "*wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source, a second signal that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor.*" (Office Action Page 3-4).

The Office Action erroneously suggests that:

> "one of ordinary skill in the art at the time of the invention would realize that the logical value of the signal applied to the gate of the transistor is a function of whether the transistor should be turned on or off and the type of transistor used. There are only a finite number of configuration the transistors can be in, either both are NMOS, both are PMOS or one is NMOS and the other PMOS. Therefore is would have been obvious to try the three possible configurations."

Applicant respectfully disagrees. Even if (but not admitted) the inventive variations were limited to the Office Actions proposed combinations, *Edwards* does not state or in any way suggest the combination of features claimed by Applicant.

Thus, *Edwards* does not disclose nor in any way suggest Applicant's claimed features of independent claim 1.

Tusuchi does not remedy the deficiencies of *Edwards*. *Tusuchi* operates either the analog buffer circuit 30 or the binary drive circuit 32 (both of which are part of the output circuit 28) in response to display mode signals sent to the output circuit 28, such that the analog buffer circuit 30 does not require idle power when the binary drive circuit is in operation the during simple display mode.

Tusuchi is relied upon for purported disclosure of an output circuit buffer that contains an analog buffer and a precharge circuit in which the analog buffer can be disconnected from the precharge circuit; however, in conjunction with the deficiencies of *Edwards*, *Tusuchi* also does not disclose "*the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period, and the buffer circuit includes an analog buffer circuit and a precharge circuit; and executing a precharge processing for the*

precharge period by disconnecting the precharge circuit for the precharge period from the analog buffer circuit, where the buffer circuit transistor of the buffer circuit is part of the analog buffer circuit."

That is, *Tusuchi* does not disclose "*the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period ... where the buffer circuit transistor of the buffer circuit is part of the analog buffer circuit*," because *Tusuchi* use of display signals to alternate between the analog buffer circuit 30 or the binary drive circuit 32 does not define a temporary connection or the location of where that connection occurs.

Accordingly, since even a combination of *Edwards* and *Tusuchi* would still fail to yield features of Applicant's claimed invention, a *prima facie* case of obviousness for independent claim 1 has not been presented.

For reasons similar to those provided for claim 1, independent claims 3 and 5 are neither disclosed, taught, or suggested by *Edwards* and *Tusuchi*. The dependent claims are also distinct for their incorporation of the features respectively recited in the independent claims as well as for their own, separately recited patentably distinct features.

Specifically, regarding claim 2, repeating the period when the voltage between terminals of the capacitor for sampling is set in not disclosed in *Edwards*.

Further, new claims 7-9 are not disclosed by *Edwards* and *Tusuchi* for their incorporation of the independent claims and for their own patentably distinct features.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over *Edwards* and *Tusuchi*.

In view of the above amendment, applicant believes the pending application is in condition for allowance. If any further issues remain, the Examiner is invited to telephone the undersigned to resolve them.

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

This response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-3056 from which the undersigned is authorized to draw.

Dated: October 27, 2011

Respectfully submitted,

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